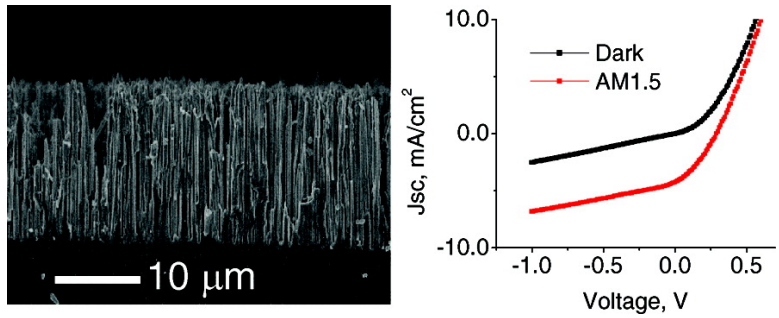
Communication

Silicon Nanowire Radial p#n Junction Solar Cells

Erik C. Garnett, and Peidong Yang

J. Am. Chem. Soc., **2008**, 130 (29), 9224-9225 • DOI: 10.1021/ja8032907 • Publication Date (Web): 25 June 2008



More About This Article

Additional resources and features associated with this article are available within the HTML version:

- Supporting Information
- Links to the 3 articles that cite this article, as of the time of this article download
- Access to high resolution figures
- Links to articles and content related to this article
- Copyright permission to reproduce figures and/or text from this article

View the Full Text HTML

J|A|C|S
COMMUNICATIONS

Published on Web 06/25/2008

Silicon Nanowire Radial p−n Junction Solar Cells

Erik C. Garnett and Peidong Yang*

Department of Chemistry, University of California, Berkeley, California 94720, and Material Sciences Division, Lawrence Berkeley National Laboratory, Berkeley, California 94720

Received May 2, 2008; E-mail: p_yang@berkeley.edu

Semiconducting nanowires have the potential to impact many different technologies either through improved material properties or by offering a new geometry not possible with bulk or thin film devices.[1−5] Solar energy is one particularly relevant application due to the rising monetary and environmental cost of fossil fuels.[6] One of the primary barriers to widespread photovoltaic (PV) use is the high PV cell production cost, nearly half of which is imbedded in the initial silicon wafer.[7,8] Although metallurgical grade silicon (mg-Si) is inexpensive at only about $1.75−$2.30/kg,[9] it has far too many impurities to yield efficient solar cells; the necessary further purification leads to a cost of about $20−30/kg for solar grade silicon (sg-Si).[10] Additionally, converting mg-Si to sg-Si is highly energy intensive, composing almost half of the total energy required for the final PV cell.[11] Relaxing the purification requirements should reduce the energy payback time considerably. Therefore, a device geometry that allows for lower purity silicon should greatly reduce the cost (both monetary and environmental) of the final PV cell and help to increase market penetration. Vertically aligned silicon nanowire solar cells (Si NW SCs) have already been shown theoretically to be much less sensitive to impurities versus planar Si SCs,[5] but there have been only limited reports testing this idea.[12−15] This paper describes the fabrication of wafer-scale arrays of n-type Si NWs with a solution-phase etching method, deposition of p-type amorphous Si (a-Si) using low pressure chemical vapor deposition (LPCVD) and subsequent crystallization with rapid thermal annealing (RTA). This yields core−shell n−p junction Si NW array SCs fabricated using only low-energy, scalable processes. The efficiency is about 0.5% at this stage, but further optimization, including surface passivation, could lead to cells with efficiencies close to bulk silicon that have a much higher defect density tolerance.

Si NW arrays were made by an aqueous electroless etching method following Peng et al.[12] Briefly, silver nitrate, hydrofluoric acid, and water were mixed and added to an open Teflon crystallizing dish along with a clean silicon wafer and heated to 50 °C in an oven for 2 h. The wafer was washed with water, and the silver was removed with concentrated nitric acid. The silicon oxide was removed with a buffered hydrofluoric acid solution and the a-Si thin film was uniformly deposited at 450 °C using disilane as the silicon source and boron trichloride as the dopant gas. The film was crystallized with RTA in forming gas at 1000 °C for 10 s, the backside p-Si was removed with a silicon wet etch, and contacts were made using sputtered Ti/Ag on the n-Si and Ti/Pd on the p-Si. The cells were tested with an Oriel solar simulator under AM1.5 illumination.

Figure 1a,b shows a schematic picture and cross-sectional scanning electron micrograph (SEM) of a Si NW n−p core−shell solar cell after the amorphous silicon LPCVD deposition and crystallization. The device shows 18 μm long nanowires with excellent vertical alignment, uniformity, and packing density, with about 50% area density, similar to previous reports using this NW

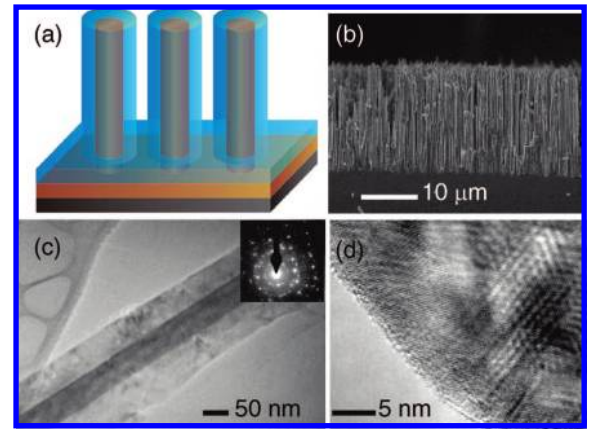


Figure 1. Silicon nanowire solar cell structure. (a) Schematic cell design with the single crystalline n-Si NW core in brown, the polycrystalline p-Si shell in blue, and the back contact in black. (b) Cross-sectional SEM of a completed device demonstrating excellent vertical alignment and dense wire packing. (c) TEM image showing the single crystalline n-Si core and polycrystalline p-Si shell. The inset is the selected area electron diffraction pattern. (d) TEM image from the edge of the core−shell nanowire showing nanocrystalline domains.

synthesis.[2,12] The typical wire diameter (including the shell) from the SEM is 350−400 nm, which gives a shell thickness of about 150 nm on top of the 50−100 nm initial nanowire core. Figure 1c shows a sample with a thinner a-Si shell that was processed in parallel with the actual devices to allow for better transmission electron microscopy (TEM) interface imaging. In this bright field image, the single crystalline core is aligned to a zone axis, leading to much stronger diffraction and thus darker contrast compared to the polycrystalline shell. The diffraction pattern in the inset also clearly shows the spot pattern associated with single crystalline silicon coming from the nanowire core aligned to the [211] zone axis,[16] along with the rings associated with the polycrystalline shell. The TEM image taken near the edge of the nanowire (Figure 1d) shows roughly 5 nm domains, indicating a nanocrystalline film. The deposition rate calculated from TEM images was 1.9 nm/min and consistent with the thickness observed in the SEM. The X-ray diffraction (XRD) patterns taken from the solar cell before and after the RTA treatment (Supporting Information) confirm the amorphous to polycrystalline transition, as well. Planar oxidized silicon wafers were processed in parallel with the solar cells in order to extract the silicon thin film electrical properties after various annealing treatments. The as-deposited boron-doped amorphous silicon film was too resistive to measure, but after RTA at 1000 °C for 10 s, the same film showed a four-point probe resistance of about 200 Ω/square. The film resistivity of 0.013 Ω·cm, doping level of 1.7 × 10^{19} cm^{-3}, and mobility of 30 $cm^2/V·s$ were extracted from Hall measurements. The phosphorus dopant concentration in the etched nanowires should be unchanged from that of the starting Si

10.1021/ja8032907 CCC: $40.75

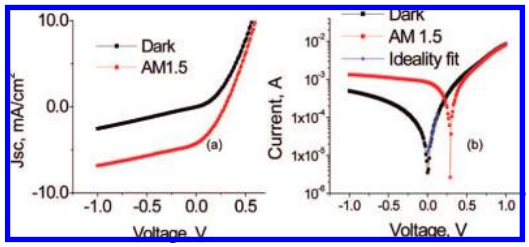


Figure 2. Silicon nanowire solar cell electrical performance. (a) Current−voltage behavior in the dark and under AM1.5 simulated sunlight irradiation. (b) Semilog plot of the same data used to extract the diode ideality factor of 2.1.

wafer, which was about 1×10^{16} cm^{-3} according to the wafer resistivity of 0.6 Ω·cm.[17]

Figure 2 shows the electrical output characteristics of a Si NW array PV. Under AM1.5 illumination, the device has an open circuit voltage (V_{oc}) of 0.29 V, a short circuit current (J_{sc}) of 4.28 mA/cm^2, and a fill factor (FF) of 0.33 for an overall efficiency of 0.46%. The low V_{oc} stems from interfacial recombination as evidenced by the large dark current and high diode ideality factor (Figure 2b).[18] The high surface to volume ratio in the nanowire arrays is expected to exacerbate recombination, making surface passivation even more important for these devices than for bulk silicon solar cells. The large surface roughness previously observed in similarly etched Si NWs[2] could also lead to enhanced depletion region traps, especially since this surface is located directly at the p−n junction in the final device. However, even smooth wires synthesized using the vapor−liquid−solid (VLS) mechanism have been shown to exhibit severe surface recombination, giving minority carrier diffusion lengths which are limited by the wire diameter.[19] Additionally, single coaxial Si NW solar cells made from smooth VLS grown wires and polycrystalline thin films showed similar values for V_{oc} and diode ideality factor.[20] However, that study found that inserting an intrinsic silicon layer between the n-Si and p-Si components was necessary to achieve even this relatively low V_{oc} value, while we did not use such a layer in our devices. It is also possible that some nanowires located underneath the contacts were broken, exposing the underlying n-Si and leading to a reduced shunt resistance, which would also give a lower V_{oc} and increased dark current.

Using the low field diode ideality factor of 2.1 and V_{oc} of 0.29, we calculated an ideal FF of 0.49, which is well above the observed value of 0.33.[18] We can reconcile these differences by including a series resistance of 110 ohms in the above FF calculation, which is close to the measured polycrystalline p-Si film resistance. This significant series resistance contribution to the fill factor is consistent with the low measured J_{sc}. The 5-fold higher J_{sc} reported for a single nanowire coaxial p−n junction solar cell[20] should not be due to absorption differences only since we have a similar nanocrystalline thin film coating on our nanowires and a much longer light absorption path length, but may be at least partially attributable to a smaller series resistance. The increased surface roughness of our Si NWs compared to that of VLS-grown wires may be one contributing factor in this resistance difference.[2] It is interesting to note that Si NW SCs fabricated using the same etching technique but with the p−n junction deep within the wafer (as opposed to within the wire) showed a much higher efficiency of up to nearly 10%.[12] This further reinforces the idea that depletion region recombination is dramatically enhanced by the close proximity of the surface to the p−n junction. Future studies will focus on limiting this interfacial recombination by passivating the surface and reducing roughness while increasing the p-Si conductivity to minimize the series resistance.

In summary, we have demonstrated a low-temperature wafer-scale etching and thin film deposition method for fabricating silicon n−p core−shell nanowire solar cells. Our devices showed efficiencies up to nearly 0.5%, limited primarily by interfacial recombination and high series resistance. Surface passivation and contact optimization will be critical to improve device performance in the future.

Acknowledgment. E.C.G. would like to thank Ben Yuhas for assistance with imaging and the Berkeley Microfabrication Laboratory and National Center for Electron Microscopy for use of their facilities. This work was supported by NSF and the Simon family fund.

Supporting Information Available: Detailed information about the nanowire synthesis, a-Si thin film deposition, RTA annealing conditions, contact formation, cell testing, and XRD. This material is available free of charge via the Internet at http://pubs.acs.org.

References

(1) He, R.; Yang, P. *Nat. Nanotechnol.* **2006**, *1*, 42–46.
(2) Hochbaum, A. I.; Chen, R. K.; Delgado, R. D.; Liang, W. J.; Garnett, E. C.; Najarian, M.; Majumdar, A.; Yang, P. D. *Nature* **2008**, *451*, 163–167.
(3) Feng, X. L.; He, R. R.; Yang, P. D.; Roukes, M. L. *Nano Lett.* **2007**, *7*, 1953–1959.
(4) Chan, C. K.; Peng, H. L.; Liu, G.; McIlwrath, K.; Zhang, X. F.; Huggins, R. A.; Cui, Y. *Nat. Nanotechnol.* **2008**, *3*, 31–35.
(5) Kayes, B. M.; Atwater, H. A.; Lewis, N. S. *J. Appl. Phys.* **2005**, *97*, 114302.
(6) Hoffert, M. I.; Caldeira, K.; Jain, A. K.; Haites, E. F.; Harvey, L. D. D.; Potter, S. D.; Schlesinger, M. E.; Schneider, S. H.; Watts, R. G.; Wigley, T. M. L.; Wuebbles, D. J. *Nature* **1998**, *395*, 881–884.
(7) Solar energy−Sunny Days Ahead? Current Status and Outlook for Photovoltaics and Solar Thermal Power. *Sarasin Sustainable Investment Report*; Fawer-Wasswer, M., November 2004.
(8) Green, M. A. *Sol. Energy* **2004**, *76*, 3–8.
(9) Silicon. *USGS Mineral Commodities Survey*; January 2008.
(10) Mauk, M. G.; Rand, J. A.; Jonceyk R.; Hall R. B.; Bamett A. M.; Solar-Grade Silicon: The Next Decade. In Proceedings of the Third World Conference on Photovoltaic Energy Conversion, Osaka, Japan, May 11–18, 2003 IEEE Publications: Los Alamitos, CA, 2003; Vol. 1, pp 939–942.
(11) Alsema, E. A. *Prog. Photovoltaics* **2000**, *8*, 17–25.
(12) Peng, K. Q.; Xu, Y.; Wu, Y.; Yan, Y. J.; Lee, S. T.; Zhu, J. *Small* **2005**, *1*, 1062–1067.
(13) Tsakalakos, L.; Balch, J.; Fronheiser, J.; Korevaar, B. A.; Sulima, O.; Rand, J. *Appl. Phys. Lett.* **2007**, *91*, 233117.
(14) Goodey, A. P.; Eichfeld, S. M.; Lew, K. K.; Redwing, J. M.; Mallouk, T. E. *J. Am. Chem. Soc.* **2007**, *129*, 12344–12345.
(15) Maiolo, J. R.; Kayes, B. M.; Filler, M. A.; Putnam, M. C.; Kelzenberg, M. D.; Atwater, H. A.; Lewis, N. S. *J. Am. Chem. Soc.* **2007**, *129*, 12346–12347.
(16) Fultz, B.; Howe, J. M. In *Transmission Electron Microscopy and Diffractometry of Materials*; Springer-Verlag: Berlin, 2002; p 748.
(17) Ghandhi, S. K. In *VLSI Fabrication Principles*; Wiley-Interscience: New York, 1983; p 664.
(18) Green, M. A. In *Solar Cells: Operating Principles, Technology and System Applications*; Prentice-Hall, Inc.: Englewood Cliffs, NJ, 1982; p 274.
(19) Kelzenberg, M. D.; Turner-Evans, D. B.; Kayes, B. M.; Filler, M. A.; Putnam, M. C.; Lewis, N. S.; Atwater, H. A. *Nano Lett.* **2008**, *8*, 710–714.
(20) Tian, B. Z.; Zheng, X. L.; Kempa, T. J.; Fang, Y.; Yu, N. F.; Yu, G. H.; Huang, J. L.; Lieber, C. M. *Nature* **2007**, *449*, 885–889.

JA8032907